Cambridge International AS & A Level

Cambridge Assessment International Education
Cambridge International Advanced Subsidiary and Advanced Level

COMPUTER SCIENCE **9608/32**

Paper 3 Written Paper **October/November 2017**

MARK SCHEME

Maximum Mark: 75

Published

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Mark schemes should be read in conjunction with the question paper and the Principal Examiner Report for Teachers.

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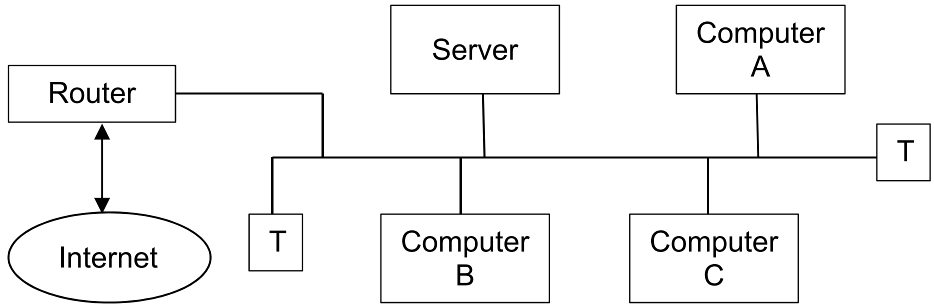
Cambridge Assessment International Education

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>1(a)</td><td>


Each device has a single connection to the bus (1)

One terminator at each end (1)

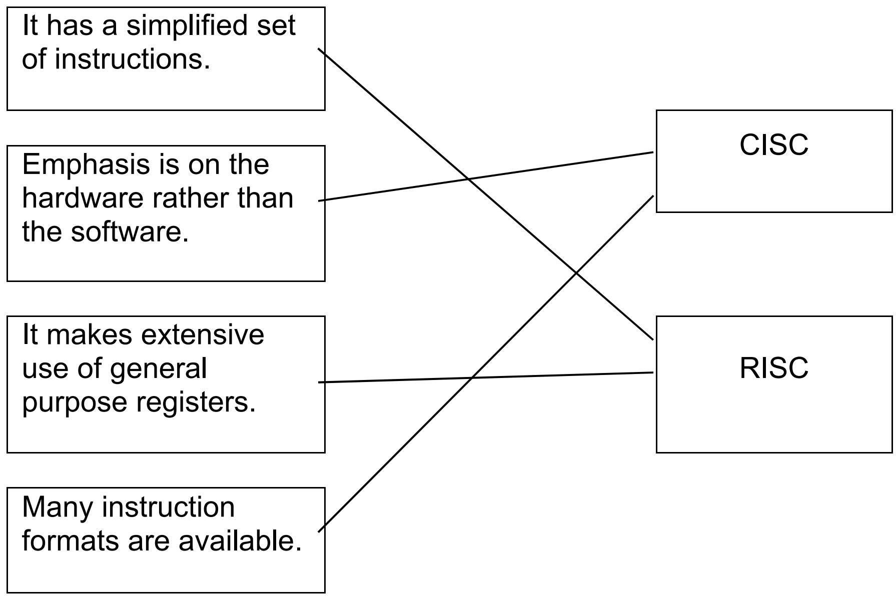
The terminators do not need to be labelled as long as they are obvious
</td><td>2</td></tr>
<tr><td>1(b)</td><td>
<table>
<tr><th>Statement</th><th>True</th><th>False</th><th></th></tr>
<tr><td>The server can send packets to Computer B and the router at the same time.</td><td></td><td>✓</td><td>(1)</td></tr>
<tr><td>Computer C uses the IP address of a web server to send a request for a web page on the web server</td><td>✓</td><td></td><td>(1)</td></tr>
<tr><td>Computer B can read a packet sent from Computer A to Computer C.</td><td>✓</td><td></td><td>(1)</td></tr>
<tr><td>The server can read all incoming packets from the Internet.</td><td>✓</td><td>✓</td><td>(1)</td></tr>
</table>
</td><td>4</td></tr>
<tr><td>1(c)(i)</td><td>
Only one transmission is allowed on the bus at <u>any one time</u> // only one packet can be transmitted on the bus at <u>any one time</u> (1)
The two packets from A and B cannot both use the bus at the same time (1)
The attempts to transmit will be unsuccessful, because the stations will realise that the bus is busy (1)
Reference to CSMA/CD (1)
Collision causes a change in voltage of the bus (1)
1 mark for each point, max 2
</td><td>2</td></tr>
<tr><td>1(c)(ii)</td><td>
One mark for valid point, max 2

Calculate a <u>random</u> wait time
Wait for the <u>random</u> time
Check for idle bus // Check status of bus
Attempt to re-transmit / re-send
If unable to transmit, repeat process
</td><td>2</td></tr>
</table>

Question	Answer	Marks
1(d)(i)	Star topology (1) Where each computer / device has its own <u>dedicated connection</u> to the server (1) Alternative answers: Mesh topology (1) Every device <u>connects</u> directly to every other device (1) Ring topology (1) Use of <u>tokens</u> means no collisions // Every device examines every packet (1)	**2**
1(d)(ii)	As each computer is now not sharing a single bus // has dedicated path (to the server) (1) Collisions <u>cannot</u> occur (1) Alternative answers: Mesh As each device now has a direct path <u>to all the others</u> (1) Collisions <u>cannot</u> occur (1) Ring Packets all travel in the same direction (1) Collisions <u>cannot</u> occur (1)	**2**

Question	Answer	Marks
2(a)	see below	4

Description **Type of processor**



1 mark for each correct line

Question	Answer	Marks
2(b)(i)	**One mark** per point – **max 2** Pipelining is instruction level parallelism Execution (A: processing) of an instruction is split into a number of stages When first stage for an instruction is completed the first stage of the next instruction can start executing Another instruction can start executing before the previous one is finished Processing of a number of instructions can be concurrent / simultaneous	2
2(b)(ii)	see below	3

Time Interval

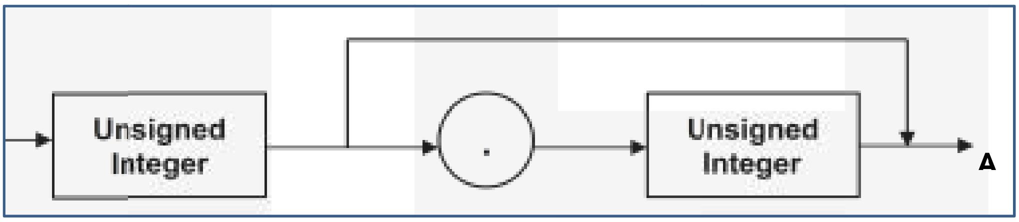
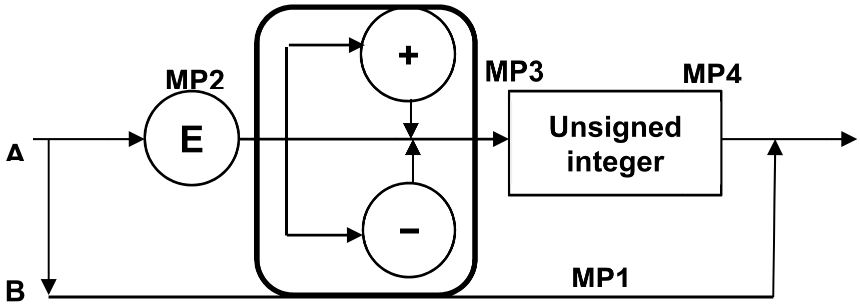
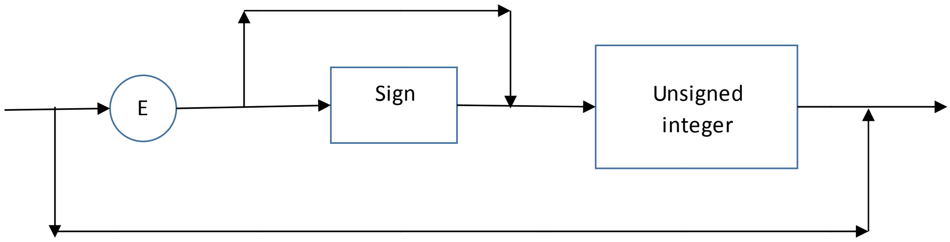
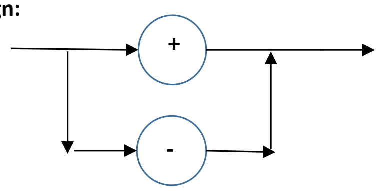
Stage	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Fetch instruction	D	**E**						
Read registers and decode instruction		D	E					
Execute instruction			D	E				
Access operand in memory				D	E			
Write result to register					D	E		

D at time interval 1 (1)
D and E in second row (in that order) (1)
Remainder completed correctly (1)

Question	Answer	Marks
2(c)(i)	**Two** from: The result of the first addition is not stored in (register) r3 (1) Before the next instruction needs to load value from r3 (1) There is a data dependency issue (1) r3 is being fetched and stored on the same clock pulse (1)	**2**
2(c)(ii)	The third instruction is not dependent on the first two, therefore, instruction 2 and 3 need to be swapped	**1**

Question	Answer	Marks
3(a)(i)	**A**: Guest (operating system) (1) **B**: Host (operating system) (1)	**2**
3(a)(ii)	**One mark** for each valid point, **max 3** Guest OS (A) handles request as if it were running on its own physical machine // guest OS (A) is not aware it is running on a virtual platform Guest OS (A) handles the request as usual I/O requests are translated by the virtual machine software Into instructions executed by host OS (B) Host OS (**B**) retrieves the data from the file Host OS (**B**) passes the data to the virtual machine software The virtual machine software passes the data to the guest OS (**A**) Guest OS passes the data to the application	**3**
3(b)(i)	**One mark** from: Because software can be tried on different OS using same hardware Because no need to purchase / request all sorts of different hardware Easier to recover if software causes system crash VM provides protection to other software / host OS from malfunctioning software	**1**
3(b)(ii)	**Max 2 marks** per limitation, **max 2** limitations – **max 4 marks** Virtual machine may not be able to emulate some hardware … So that hardware cannot be tested using a virtual machine … By relevant example, e.g. developing hardware drivers Using virtual machine means execution of extra code // processing time increased … so cannot accurately test speed of real performance A virtual machine might not be as efficient … By relevant example, e.g. might not be able to access sufficient memory	**4**

Question	Answer	Marks
4(a)(i)	Because a valid unsigned integer can be two digits / one or more digits (1) Both 3 and 2 are digits (1)	**2**
4(a)(ii)	Because a valid unsigned number can be an unsigned integer followed by a decimal point followed by an unsigned integer (1) 32 is an unsigned integer and 5 is an unsigned integer (because it is a digit) and there is a point in between (1) Alternative response for 2 marks, combination of order and validity: 32 is a (valid) unsigned integer, followed by a decimal point, and 5 which is another (valid) unsigned integer Validity mark must refer to 32 and 5	**2**
4(b)	<unsigned number> ::= **<unsigned_integer> |** (1) **<unsigned_integer>.<unsigned_integer>** (1) Accept order reversed: <unsigned_integer> ::= **<digit> |** (1) **<digit> <unsigned_integer>** (1) Accept **<digit> |<unsigned_integer> <digit>** If order reversed mark as above <digit> ::= **1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0** (1) Accept the list in any order, as long as all 10 digits included	**5**

Question	Answer	Marks
4(c)(i)	  **MP1**: Line to indicate exponent is optional (B line) (1) **MP2**: 'E' present at start of exponent (1) **MP3**: Optional '+' or '-' (1) **MP4**: Unsigned integer (1) Alternative correct answer: MP3 needs both the sign 'box' and the sign diagram for the mark  **Sign:** 	4

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>4(c)(ii)</td><td><unsigned number> ::=
<unsigned_integer >
| <unsigned integer>.<unsigned_integer> (1)

Accept any order

| <unsigned_integer > <exponent>
| <unsigned integer>.<unsigned_integer> <exponent> (1)

Accept any order

<exponent> ::= E <sign> <unsigned_integer>
| E <unsigned integer> (1)

<sign> ::= + | - (1)</td><td>4</td></tr>
</table>

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>5(a)</td><td>
<table>
<tr><th>A</th><th>B</th><th>X</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>1</td></tr>
<tr><td>5(b)</td><td>
<table>
<tr><th></th><th>S</th><th>R</th><th>Q</th><th>$\overline{Q}$</th><th></th></tr>
<tr><td>Initially</td><td>1</td><td>0</td><td>1</td><td>0</td><td></td></tr>
<tr><td>S changed to 0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>(1)</td></tr>
<tr><td>R changed to 1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>(1)</td></tr>
<tr><td>R changed to 0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>(1)</td></tr>
<tr><td>S and R changed to 1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>(1)</td></tr>
</table>
</td><td>4</td></tr>
<tr><td>5(c)(i)</td><td>Clock (pulse)</td><td>1</td></tr>
<tr><td>5(c)(ii)</td><td>Max 2 marks per problem – max 4 marks

Problem 1
One combination of S and R gives NOT valid / indeterminate output // Q and $\overline{Q}$ have the same value
The JK flip-flop does not allow for Q and $\overline{Q}$ to have the same value for any combination of inputs // $\overline{Q}$ and Q have to be complementary

Problem 2
Inputs may not arrive at the same time
The JK flip-flop has a clock pulse to synchronise inputs</td><td>4</td></tr>
</table>

Question	Answer	Marks
6(a)	**One mark** for suitable sensor, **one mark** for justification **Max one sensor, max two marks** humidity … to ensure that the plants have the right level of moisture in the air pressure / proximity … to detect whether the windows are open or closed condone '*check*' moisture … to ensure the water levels in the soil are correct light … to ensure the light levels in the greenhouse are correct for plant growth … to ensure the windows are closed when night falls Accept pH sensor for one mark only Accept CO_2 sensor for one mark only, accept gas or O_2 for one mark only Justification needs to answer the question why? Not just describe the sensor Accept suitable actions resulting from sensor readings as justification	**2**
6(b)	**Three** from: Actions taken by system // or by example: e.g. adjust heater / turn on sprinkler / open windows May affect the readings taken by the sensors // or by example Which in turn may cause a change in the actions taken by the system // or by example This is a continuous process…	**3**
6(c)(i)	**One** from: Lowest allowable temperature Highest allowable temperature Sampling time interval	**1**

Question	Answer	Marks
6(c)(ii)	If answer to **c(i)** is **highest allowable or lowest allowable temperature**: The sensor reading is compared to a stored parameter (1) Depending upon result of comparison an action may or may not be carried out (1) If answer to **c(i)** is **sampling time interval**: The higher the sampling rate… (1) …The better / more efficient is the control system (1)	**2**
6(d)(i)	20	**1**
6(d)(ii)	`LDD` **`4002`** `// load the contents of the 16 bit location containing the value for Sensor 5 into the Accumulator` **`LSR #8`** `// move the bits in the Accumulator so that the Accumulator stores the value of Sensor 5 as unsigned 16-bit binary integer` 1 mark for 4002 1 mark for LSR 1 mark for #8	**3**